

REMARKS

Claims 1-4, 6-10, 12-15 and 40 are pending. Claims 1, 9 and 40 are currently amended. Support for the amendment is detailed below. Applicants' undersigned representative thanks Examiner Le for the courtesies extended during the telephone interview of August 14, 2006. Applicants' separate record of the substance of the interview is incorporated below.

Applicants' Response to the Claim Rejection under 35 U.S.C. §103:

Claims 1-4, 7, 9-10, 12, 14 and 40 stand rejected under 35 U.S.C. 103 as being unpatentable over US 6544845 to **Yoo et al.** (hereinafter "**Yoo**") in view of US 6294430 to **Fastow et al.** (hereinafter "**Fastow**"). In response thereto, applicants have amended claims 1, 9 and 40 to more distinctly claim the subject matter regarded as the invention. Specifically, applicants have included the feature that the gate insulating film which is interposed between that substrate and the second gate electrode has a uniform thickness through out the entire length of the gate electrode. As illustrated in Fig. 10B, of the current application, the thermal oxide film 12B is completely uniform underneath the entire gate electrode.

As discussed in the course of the interview, FIG. 9C illustrates that when the thermal oxidation film 18 is formed on the device, the logic circuit device area is covered with amorphous silicon 16 and the gate electrode is not yet patterned. See page 21, lines 5 to 13. In the flash memory area of the device, the gate/tunnel electrode areas are already formed, and the thermal oxide film 18 penetrates the side areas to cause birds' beak. See FIG 10A. Applicants respectfully submit that Yoo does not teach nor suggest that the gate oxide film beneath the gate

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electrode of the logic circuit transistors is entirely uniform as set forth in amended claims 1, 9 and 40.

As discussed during the interview, although Yoo states that there is no birds' beak formed in the peripheral circuit area, Yoo also states that: "... the lower portion of the edge of the peripheral circuit gate 508B of the peripheral circuit region is thermally oxidized and rounded as shown in the circle marked with the R2 through the above-mentioned thermal processing." See column 9, lines 11-14 and FIG. 11(b). Hence, Yoo does not teach a uniform surface of the gate oxide layer underneath the entire gate electrode. Yoo requires the rounding of the corners R2 of the gate oxide which is formed by exposing the peripheral circuit region to thermal oxidation.

In view of the aforementioned amendments and accompanying remarks, Applicants submit that the claims, as herein amended, are in condition for allowance. Applicants request such action at an early date.

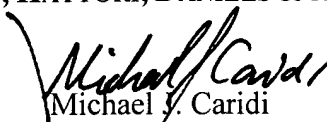
If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

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If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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